Hardware Accelerated Collision Detection
– An Architecture and Simulation Results

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What is Collision Detection?
Applications
Bounding Volumes enclose ALL volumes on lower levels of the hierarchy and can be checked for collision fastly.
Hierarchical Collision Detection
A DOP consists of $k/2$ pairs of antiparallel hyperplanes with fixed orientation.
Check For Overlap

If one slab-pair does not overlap the DOPs are not intersecting.
Enclosing DOP

To check for intersection DOP $d$ is enclosed with another DOP $d'$ with the same orientations as $e$. 
Rotation and translation

\[
\begin{pmatrix}
    d'_0 \\
    d'_1 \\
    d'_2 \\
    \vdots \\
    d'_{k-3} \\
    d'_{k-2} \\
    d'_{k-1}
\end{pmatrix}
= 
\begin{pmatrix}
    0 & 0 & C_{10} & 0 \ldots & 0 & 0 & C_{11} & C_{12} \\
    C_{20} & 0 & C_{21} & 0 \ldots & 0 & C_{22} & 0 & 0 \\
    0 & C_{20} & 0 & 0 \ldots & 0 & C_{21} & C_{23} & 0 \\
    \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\
    C_{20} & C_{21} & 0 & 0 \ldots & 0 & 0 & C_{22} & 0 \\
    0 & C_{20} & C_{21} & 0 \ldots & 0 & C_{22} & 0 & 0 \\
    0 & 0 & C_{20} & C_{21} & 0 & C_{22} & 0 & 0
\end{pmatrix}
\times
\begin{pmatrix}
    d_0 \\
    d_1 \\
    d_2 \\
    \vdots \\
    d_{k-3} \\
    d_{k-2} \\
    d_{k-1}
\end{pmatrix}
+ 
\begin{pmatrix}
    c_0 \\
    c_1 \\
    c_2 \\
    \vdots \\
    c_{k-3} \\
    c_{k-2} \\
    c_{k-1}
\end{pmatrix}
\]
DOP Transformation Unit

\[ \tilde{d}'_i = d_k C_{i_0} + d_m C_{i_1} + d_n C_{i_2} + c_i + e_{i+k/2} \]

FP MUL \rightarrow FP MUL \rightarrow FP MUL \rightarrow FP ADD

FP ADD \rightarrow FP ADD \rightarrow FP ADD

=> further refinement into 15 pipeline stages
The DOP Testing Unit

A multiplexer routes the d’s to the corresponding transformation unit in the criterion checker.

24 transformations and slap-overlap tests

NOR

If the DOPs intersect the next level of the hierarchy is fetched from memory. If a leaf is reached the according triangles are checked for intersection.
The Triangle Intersection Test (T_CHECK) consists of 52 pipeline stages.
Benchmark

- Converge two identical objects
- Rotate one
- Average time for every distance to find all intersecting triangles
Benchmarking Results

Software version running on a 1GHz Pentium 3

VHDL-Simulation targeting a NEC CMOS ASIC (CB-130 UX5, 800 MHz) running at 266MHz

Door Latch
Software Collision Testing

Door Latch
Hardware Collision Testing

Time to find all intersecting triangles

µSec

#Triangles

Distance

0 1008
1502
3004
7010
12624
20898
26136
43509
80989

0.6 0.66 0.73 0.79 0.85 0.92

0 1 1.5 2 2.5 3 3.5 4

0.6 0.66 0.73 0.79 0.85 0.92

0 1008
1502
3004
7010
12624
20898
26136
43509
80989

Speed-Up of serveral orders of magnitude
Future Work

- Implementation on an FPGA
- Comparison of different Bounding-Volumes
- Compression of Bounding-Volume Hierarchy in Memory
- Hardware collision-testing of different primitives
- Further investigation in different traversal strategies
Summary

- Design of
  - a DOP intersection test hardware
  - a triangle intersection test hardware
  - a control-unit
- Simulation in VHDL
- Benchmarks
  - of complete design
  - of different traversal strategies

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