

Hardware Accelerated Collision Detection using Bounded-Error Fixed-Point Arithmetic

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Computer-Graphic ²

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Technical Computer
Science ¹



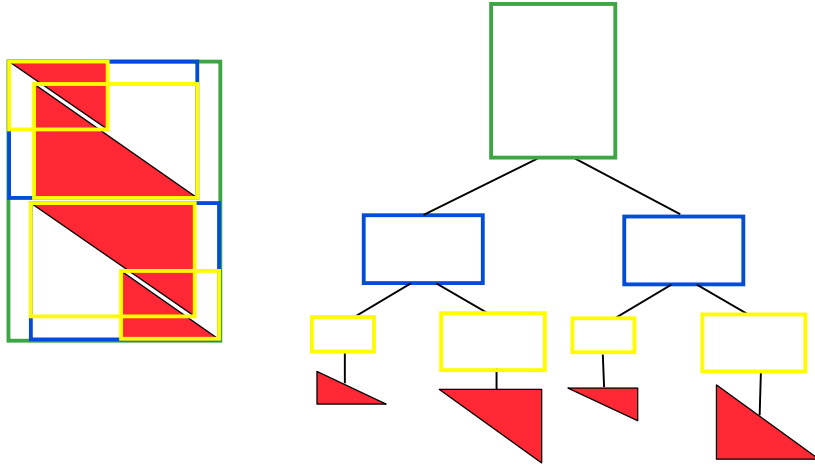
universität**bonn**

DFG-Project CollisionChip ZA292/2-1
www.collisionchip.de

What is Collision Detection?



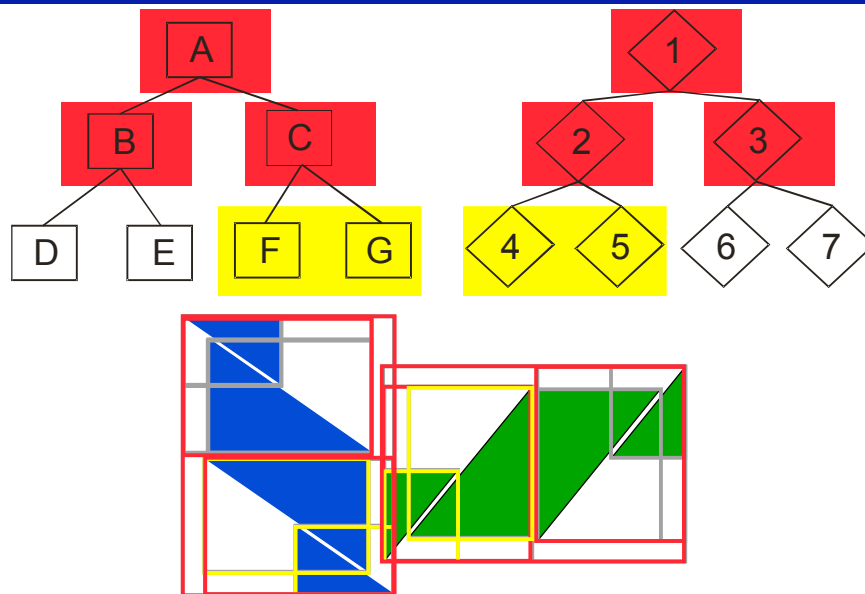
Bounding-Volume Hierarchy



Bounding Volumes enclose ALL volumes on lower levels of the hierarchy and can be checked for collision fastly.

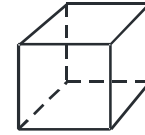
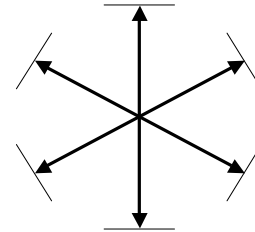
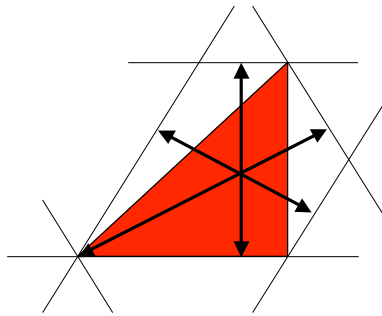
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Hierarchical Collision Detection



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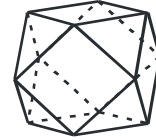
k-DOPs



6-DOP



8-DOP



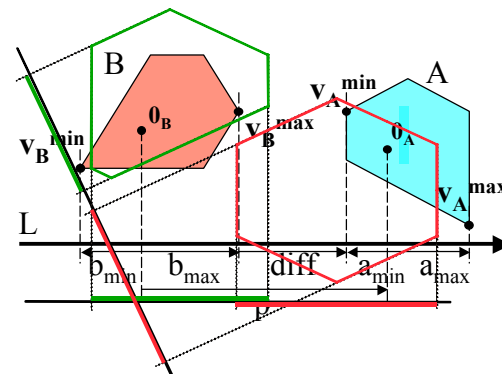
14-DOP

A DOP consists of $k/2$ pairs of antiparallel hyperplanes with fixed orientation.

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Separating Axis Test (SAT)

- SAT-Algorithm:
 - Choose Testaxis L
 - Project onto L
 - Intervals are separated
=> BVs are separated



- Mathematics:

$$a_{\min} = v_A^{\min} \cdot L$$

$$a_{\max} = v_A^{\max} \cdot L$$

$$\text{diff}_1 = (a_{\min} + p) - b_{\max}$$

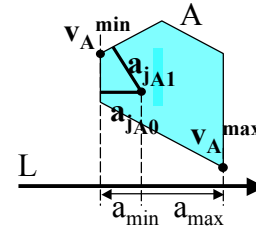
$$\text{diff}_2 = b_{\min} - (a_{\max} + p)$$

$$\text{Separation on L: } 0 < \text{diff} = \max(\text{diff}_1, \text{diff}_2)$$

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SAT for k-DOPs

- **Individual:**
 - DOP-Coefficients a_i
- **Identical within Hierarchy:**
 - Orientations A_i
 - Correspondencies j_A (A_i of v_A^{\min})



- **Mathematics:**

$$v_A^{\min} = (a_{j_{A0}} \ a_{j_{A1}} \ a_{j_{A2}}) \cdot (A_{j_{A0}} \ A_{j_{A1}} \ A_{j_{A2}})^{-1}$$

$$a_{\min} = v_A^{\min} \cdot L$$

$$= (a_{j_{A0}} \ a_{j_{A1}} \ a_{j_{A2}}) \cdot (A_{j_{A0}} \ A_{j_{A1}} \ A_{j_{A2}})^{-1} \cdot L$$

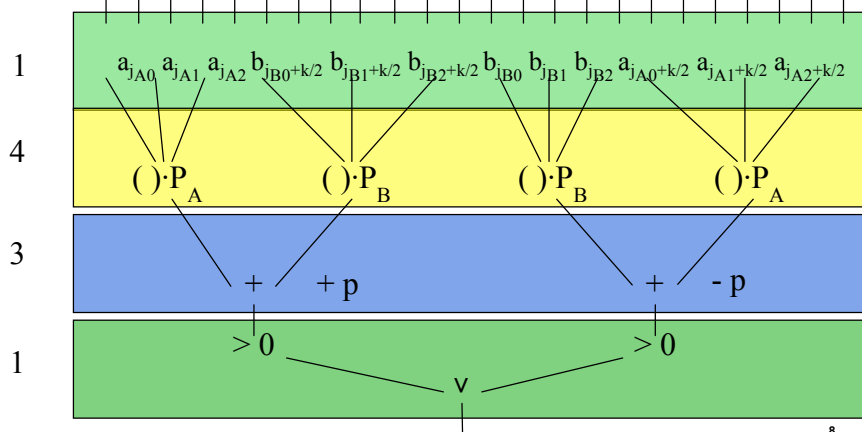
$$= (a_{j_{A0}} \ a_{j_{A1}} \ a_{j_{A2}}) \cdot P_A$$

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SAT for k-DOPs (2)

- $\text{diff}_1 = (a_{\min} + p) - b_{\max}$
- $= (a_{j_{A0}} \ a_{j_{A1}} \ a_{j_{A2}}) \cdot P_A + (b_{j_{B0+k/2}} \ b_{j_{B1+k/2}} \ b_{j_{B2+k/2}}) \cdot P_B + p$

Mikrostages



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Floating-Point vs. Fixed-Point Arithmetic

Floating-Point

- Large

- Large

+ High

Circuit Size

Development overhead

Accuracy

Fixed-Point

+ Small

+ Small

- Low

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Fixed-Point (Calculation)

- Rounding of data**

$$p - p' \leq 2^{-z}$$

$$a_i' - a_i \leq 2^{-b}$$

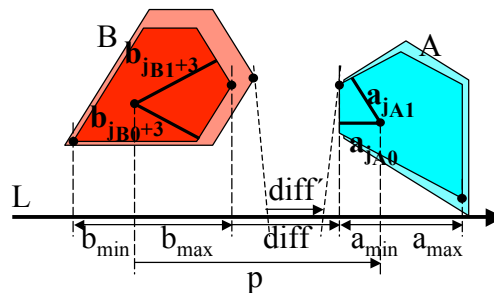
$$P_{Ai} - P_{Ai}' \leq 2^{-c}$$

- No „false negatives“:**

$$\text{diff}_1 = (a_{jA0} \ a_{jA1} \ a_{jA2}) \cdot P_A + (b_{jB0+k/2} \ b_{jB1+k/2} \ b_{jB2+k/2}) \cdot P_B + p$$

$$\text{diff}_1' = (a_{jA0}' \ a_{jA1}' \ a_{jA2}') \cdot P_A' + (b_{jB0+k/2}' \ b_{jB1+k/2}' \ b_{jB2+k/2}') \cdot P_B' + p' + \text{SN}(a_{jA0}' \ a_{jA1}' \ a_{jA2}') \cdot 2^{-c} + \text{SN}(b_{jB0+k/2}' \ b_{jB1+k/2}' \ b_{jB2+k/2}') \cdot 2^{-c}$$

- Possible error becomes larger (more „false positives“)**



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Fixed-Point (Error-Bound)

- **Error-Bound**

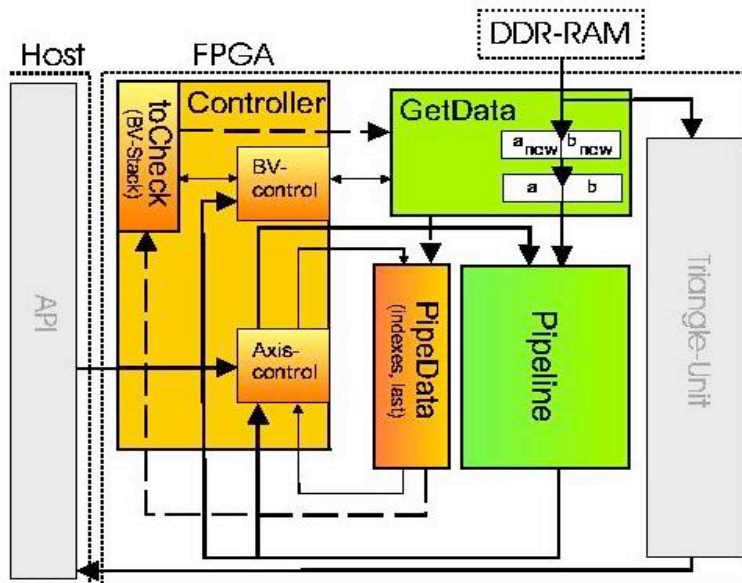
- Assumption: no acute angles between DOP-faces

$$err := diff - diff'$$

$$0 \leq err \leq \sqrt{3} \cdot 2^{-b+1} + 6 \cdot 2^{-c} + 2^{-z}$$

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Architecture



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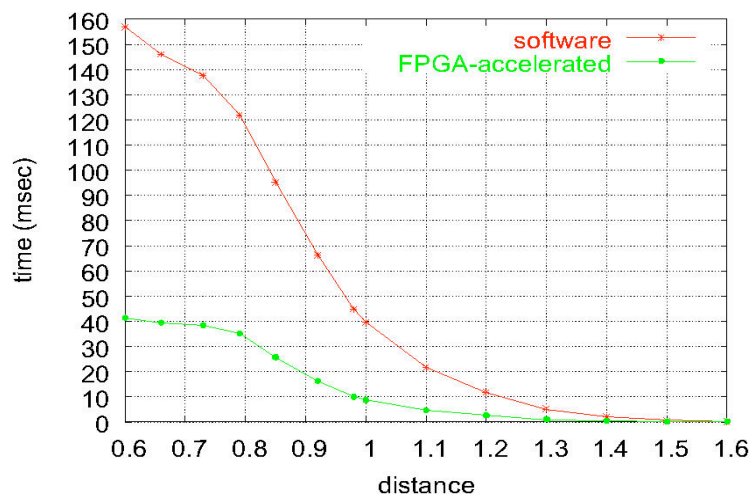
Benchmark



- Converge two identical objects
- Rotate one
- Average time to find all intersecting triangles for every distance

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Benchmark



- FPGA-Implementation has no cache
- Using FPGA-Accelerator CPU is nearly completely idle

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Future Work

- **SAT-Pipeline**
 - Determine optimal choice of parameters
- **Primitives**
 - Triangles
 - Quadrangles
 - NURBS
- **Memory-Interface**
 - Cache
 - Data-Compression
- **Deformable Objects**

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